EP 23555 (1)

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
12 July 2001 (12.07.2001)

PCT

(10) International Publication Number
WO 01/50658 A1

(51) International Patent Classification[7]: H04J 11/00

(21) International Application Number: PCT/IT00/00469

(22) International Filing Date:
21 November 2000 (21.11.2000)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
MI99A002746 30 December 1999 (30.12.1999) IT

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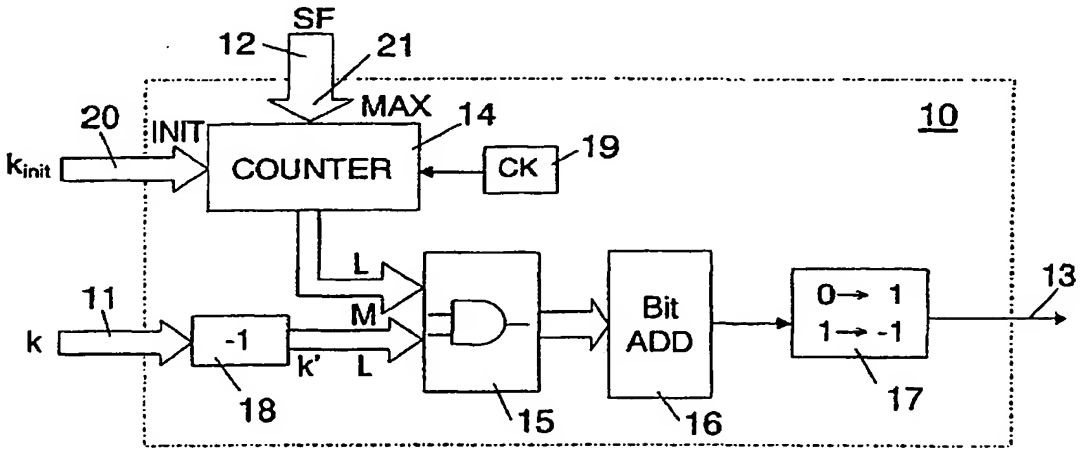
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published:
— *With international search report.*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: PROGRAMMABLE GENERATOR OF ORTHOGONAL VARIABLE SPREADING FACTOR (OVSF)



(57) Abstract: A generator for variable length orthogonal spreading sequences with maximal length 2^k and spreading factor SF is composed by an input (11) for a k bits index, which assume values in the range 0..SF-1, a binary counter (14) with a k bits output, an apparatus (15) with two k bits inputs which combine in logical AND bit by bit the two inputs in reverse order, an adder (16) that sum "modulo 2" the output of the apparatus. As the counter runs, the adder generates a sequence of bits that represent the desired sequence. This sequence should be eventually transformed from binary to polar to obtain a ±1-valued sequence.

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PROGRAMMABLE GENERATOR OF ORTHOGNAL VARIABLE SPREADING FACTOR (OSVSF)

The present invention relates to an innovative generator for orthogonal variable spreading factor (OVSF) codes.

In the spectrum division communication systems, like CDMA systems used in cellular telecommunications, the communications between base stations and mobile stations are established using the so-called "spreading codes". Substantially, the base station assigns a given number of channels to each mobile station. The distinction between the channels is given by a spreading code, which identify the specific channel. It is known to be necessary to use orthogonal variable spreading factor codes to improve the efficiency of the bandwidth usage. Since different services require different spreading factors, it is necessary to generate orthogonal variable spreading factor sequences in the physical channels. Since the code generators must be in the mobile stations too, it is important to have simple and not encumbering generators.

The objective of the present invention is to give an orthogonal variable spreading factor codes generator with a simple and reliable structure.

With this objective in mind, we have thought to realise, as described in the invention, an orthogonal variable spreading factor sequences generator with maximal length 2^k and spreading factor SF, composed by an input for a k bits index, which assume values in the range 0..SF-1; a binary counter with a k bits output; an apparatus with two k bits inputs and a k bits output which combine in logical AND bit by bit in reverse order the two inputs, connected respectively to the index input and the counter output; an adder that sum "modulo 2" the output of the apparatus. The adder output is a 0-1 sequence that represents the desired sequence generated as the counter runs.

To make clear the innovations in this invention and the advantages on the prior art, in the following will be described, with the help of the enclosed picture, a possible implementation of these principles.

In the picture is shown a generator, generally indicated with 10, that receives a given index at an input 11, a spreading factor SF at another input 12 and generate an orthogonal variable spreading factor sequence at the output 13. The generator is essentially based on a circuit including a binary counter 14 (feed by a clock generator 19), an apparatus 15 that combines the index and the output of the counter as will be explained in the following, a modulo 2 adder 16. The output of the adder will be a 0/1

sequence, to whom will be eventually applied a binary to polar translator 17 to obtain a +1/-1 sequence.

The counter should take advantage from an initialisation input 20 to which an index in the range $0..2^k$ -1 from where it is desired to start the generation of the sequence and a maximum count index 21 in which the maximum number to reach will be given.

If the indexes will assume values in the range from 1 to SF, the index input 11 will be initially decremented in a block 18 that will subtract 1 to the input before use it in the subsequent elaboration, so that it will be in the range 0..SF-1.

As is shown in the figure, the input code index (eventually decremented by 1) will be given to the block 15. Here it will be combined bit by bit in reverse order with the output of the counter, so that the less significance bit (L) of the index will be combined with the most significance bit (M) from the counter; the second less significance bit of the index will be combined with the second most significance bit from the counter, and so on. The combination will be done with a logical AND. The bits so obtained will be added modulo 2 to give only one bit in output. If necessary, this bit will be transformed in the block 17 to assume +1 or -1 values.

Typically the counter will start from 0 to count to SF-1. To establish an upper limit to the counting process, the value SF received at the input 12 will be loaded as the upper limit in the counter.

To explain the process with an example, suppose to need to generate the sequence identified by SF=16 and k=6. If the index is assuming values in the range from 1 to SF, the decrement block 18 will produce a new index k'=5, that will be binary represented as 0101. The number of bits used for the binary representation of k' and the output of the counter is given by $\log_2$ SF, in this example four bits. To generate codes with maximal length $SF_{Max}=2^k$ a k bits counter and a k elements adder will be enough. In practice, the counter and the adder will be dimensioned to be able to generate codes of the maximal length desired.

The index k'=0101 is combined in AND bit by bit to the counter output, which vary from 0000 to 1111 (binary version of SF-1=15 in decimal). The result of this combination is added modulo 2 in the block 16 and the resulting bit is transformed in the block 17 to obtain the sequence at the output 13.

The following table makes clear the overall process:

Code k'	Counter Lbit..Mbit	AND	Bit ADD	Output sequence
0101	0000	0000	0	1
	1000	0000	0	1
	0100	0100	1	-1
	1100	0100	1	-1
	0010	0000	0	1
	1010	0000	0	1
	0110	0100	1	-1
	1110	0100	1	-1
	0001	0001	1	-1
	1001	0001	1	-1
	0101	0101	0	1
	1101	0101	0	1
	0011	0001	1	-1
	1011	0001	1	-1
	0111	0101	0	1
	1111	0101	0	1

In the preceding example we have supposed to start counting from 0000, so generating a sequence from his first element. It is possible to generate a sequence starting from any element, simply initialising the counter with the index of the desired element k_{init} (assigning 0 to the first, 1 to the second, and so on).

Now it is clear how we have reached our objective, giving a circuit that allows, with a small number of components, to produce sequences of spreading codes given the code index and the spreading factor.

To everyone skilled in this art it is clear from the above description the possible practical use and the hardware that may be used to realise in practice the schema depicted in the figure. It is clear too that the method saves memory considerably with respect of the standard generation made recursively using a tree structure and requires a lower computational complexity.

Obviously the preceding description of an instance using the innovative rules of this invention is only an exemplification of these innovative rules and therefore is not a limitation of their applicability. For example if the index k is numbered from 0 to SF-1 and not from 1 to SF, the input value k will be given directly in input to the AND block 15, without any decrement. If the maximum value for the counter is fixed and invariable, the input 12 could be deleted and the counter realised to only up to this maximum value. In the same way the input 20 could be deleted if it is not desired to have the possibility to decide the starting point of the sequence.

Claims

1. Orthogonal variable spreading sequences generator with maximal length 2^k and spreading factor SF, composed by an input for a k bits index, which assume values in the range 0..SF-1; a binary counter with a k bits output; an apparatus with two k bits inputs and a k bits output which combine in logical AND bit by bit in reverse order the two inputs, connected respectively to the index input and the counter output; an adder that sum "modulo 2" the output of the apparatus. The adder output is a 0-1 sequence that represents the desired sequence generated as the counter runs.

2. A generator, as set forth in claim 1, wherein the counter has an initialisation input which allows to start counting from any value k_{init} in the range from 0 to 2^k-1.

3. A generator, as set forth in claim 1, wherein the input index is initially decremented in a block that subtract 1, so to allow the index to be in the range from 1 to SF instead in 0..SF-1.

4. A generator, as set forth in claim 1, wherein the output of the modulo two adder is connected to a block that transform from binary to polar co-ordinates, that change from 0 to 1 and from 1 to -1 the bits in the output sequence so to have a sequence that assumes only +1 or -1 values.

5. A generator, as set forth in claim 1, wherein the counter has an input to decide the maximum value to count, the spreading factor SF desired is applied to this input.

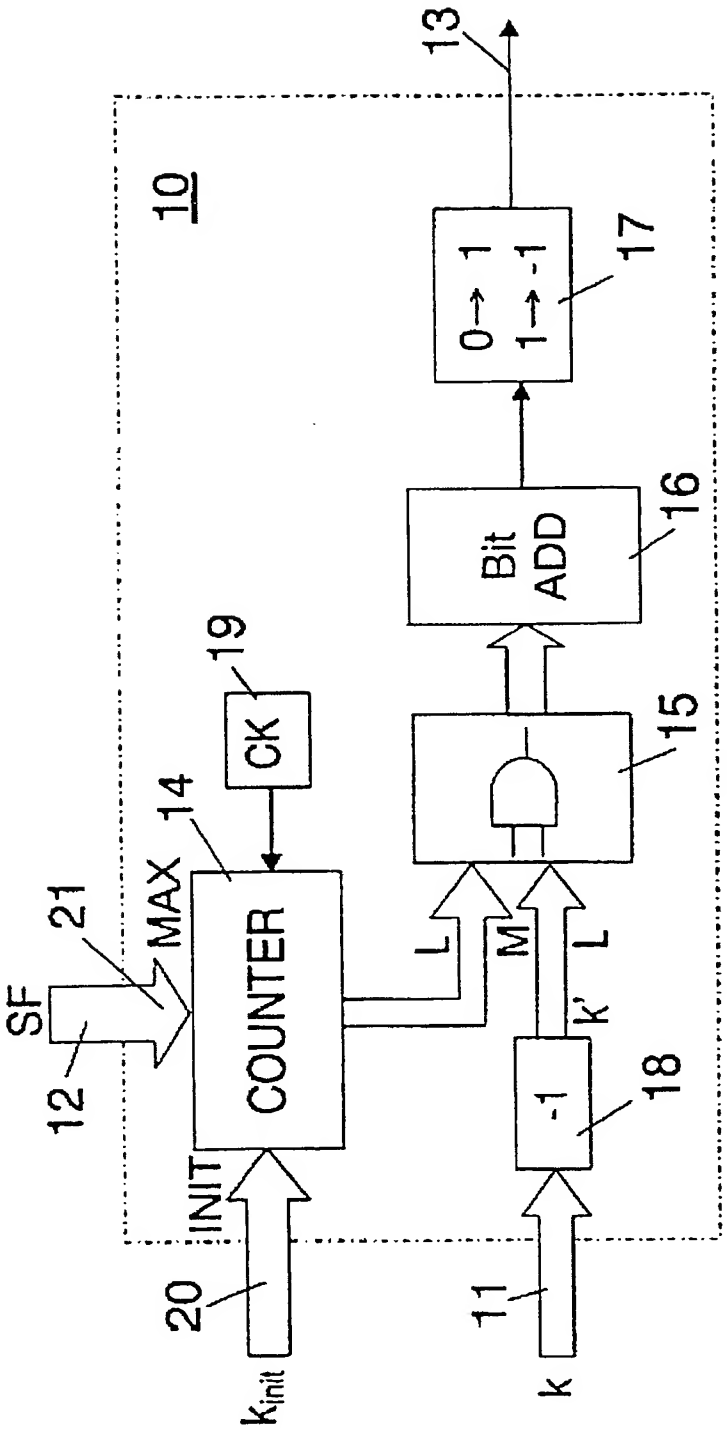

FIG. 1

INTERNATIONAL SEARCH REPORT

Int :onal Application No
PCT/IT 00/00469

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04J11/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H04J H04B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, INSPEC, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 95 03652 A (QUALCOMM INC) 2 February 1995 (1995-02-02) page 22, line 13 - line 33 figure 6	1
A	---	2-5
A	OKAWA K ET AL: "ORTHOGONAL MULTI-SPREADING FACTOR FORWARD LINK FOR COHERENT DS-CDMAMOBILE RADIO" IEEE INTERNATIONAL CONFERENCE ON UNIVERSAL PERSONAL COMMUNICATIONS,US,NEW YORK, IEEE, vol. CONF. 6, 12 October 1997 (1997-10-12), pages 618-622, XP000777896 ISBN: 0-7803-3777-8 page 620, left-hand column, line 2 - line 13 figure 4	1

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
7 March 2001	15/03/2001

Name and mailing address of the ISA	Authorized officer
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Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

Int ional Application No
PCT/IT 00/00469

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 9503652 A	02-02-1995	AU 7368294 A	20-02-1995
		IL 110373 A	06-12-1998
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		ZA 9405260 A	27-02-1995